

ABSTRACT

Disclosed herein is an SRAM-compatible memory for correcting invalid output data using parity and a method of driving the same. In the SRAM-compatible memory, input data and a parity value obtained from the input data are written in data banks and parity bank, respectively. When invalid data is output from a specific memory bank due to the performance of a refresh operation or other factors, the invalid data are corrected by a data corrector using the parity value written in the parity bank, thus generating output data having the same logic value as the input data. The SRAM-compatible memory prevents a reduction in operation speed due to an internal operation, such as a refresh operation.